


B: Amendments to The Claims:

1        1. (Currently Amended) A method for providing an area  
 2        optimized binary orthogonality checker ~~for a scalable~~  
 3        ~~selector system for controlling data transfers and routing~~  
 4        ~~in a data processing system~~ comprising the steps of:

5        determining ~~the~~ a logical gate count for an implementation  
 6        of an optomized orthogonality checker for a scalable  
 7        selector system for controlling data transfers and routing  
 8        in a data processing system; and minimizing the logical  
 9        gate count and an implementation of said orthogolality  
 10       checker given a library of logical gates to implement a  
 11       minimized circuit and ~~the~~ given an area for each logical  
 12       gate in the library and to optomize an hierarchical  
 13       orthogonality structure for said hierarchical design of  
 14       said circuit while maintaining a hierarchical design for a  
 15       circuit.

1        2 (Currently Amended) The method according to claim 1  
 2        including the steps of: establishing an optimal mix of  
 3        hierarchical level; and determining ~~the~~ inputs to implement  
 4        said orthogonality checker for said minimized circuit.

1        3. Currently Amended) The method according to claim 1,  
 2        where the area of said orthogonality checker is implemented  
 3        in ~~a~~ static CMOS circuits by minimizing the logical gate  
 4        count and an area needed for checker implementation given a  
 5        library of logical gates to implement the circuit and the  
 6        area ~~for~~ of each gate in the library.

IBM  
CORPORATION  
ARMONK, N.Y.

1 4. (Previously Amended) The method according to claim 3,  
2 including a step of establishing an optimal mix of  
3 hierarchical levels and inputs to implement said  
4 orthogonality checker to achieve said minimized circuit.

1 5. (Previously Amended) The method according to claim 4  
2 wherein said orthogonality checker is employed in a  
3 scalable selector system for controlling data transfers and  
4 routing in a data processing system, comprising a plurality  
5 of input data buses coupled to a multiple-bit, multiple bus  
6 selector having data, data valid, and an outputs of  
7 orthogonality checker and having multiple data input bus  
8 ports coupled for receipt of signal from said plurality of  
input data buses.

1 6. (Currently Amended) A method employed in a data  
2 processing system having a plurality of input data buses  
3 coupled to a multiple-bit, multiple bus selector having  
4 data, data valid, and outputs of an orthogonality checker  
5 and having multiple data input bus ports coupled for  
6 receipt of signal from said plurality of input data buses  
7 comprising the steps of:

8 establishing an expected number for a logical gate count  
9 ~~for~~ of an implementation of an orthogonality checker, and  
10 providing binary orthogonality checking by hierarchically  
11 combining the outputs of said orthogonality checker with  
12 smaller numbers of inputs and by performing ~~the~~ a total  
13 check of a large number of inputs with less gates and in a  
14 smaller area.



1 7. (Currently Amended) The method according to claim 6  
2 wherein after determining an expected number for the  
3 logical gate count, then providing multiple checks are  
4 combined with reduced input sets ~~are combined~~ into one  
5 larger check and orthogonality checking is performed, with  
6 a check on each input set, as well as with combining an OR  
7 of all the inputs for providing resulting OR values to the  
8 one larger check.

1 8. (Currently Amended) The method according to claim 7  
2 wherein the resulting OR values are then checked for  
3 orthogonality, and ~~the~~ results of all the checks are Ored  
4 together.

1 9. (Currently Amended) The method according to claim 8  
2 wherein said orthogonality checker is extended to multiple  
3 hierarchical levels and works with orthogonality checks for  
4 an extended size of implementation.

1 10. (Previously Amended) The method according to claim 9  
2 wherein the orthogonality checker has an optimal  
3 hierarchical structure for a given technology library and a  
4 given number of inputs to check.